WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a heat sink having opposed top and bottom surfaces and defining a peripheral edge;

a semiconductor die attached to the top surface of the heat sink;

a plurality of leads extending at least partially about the semiconductor die, the semiconductor die being electrically connected to at least one of the leads;

at least one first ground lead attached to the top surface of the heat sink between the semiconductor die and the peripheral edge of the heat sink;

at least one second ground lead attached to the top surface of the heat sink and protruding beyond the peripheral edge thereof;

a plurality of ground wires conductively connecting the semiconductor die, the first and second ground leads, and the heat sink to each other; and

a package body at least partially encapsulating the heat sink, the semiconductor die, the leads, the first and second ground leads, and the ground wires such that at least portions of the second ground lead and the leads are exposed in the package body.

2. The semiconductor package of Claim 1 wherein:

the first ground lead is secured to the top surface of the heat sink by a first insulating layer; and

the second ground lead is secured to the top surface of the heat sink by a second insulating layer.

3. The semiconductor package of Claim 2 wherein the first and second insulating layers are each fabricated from a polyimide tape.

4. The semiconductor package of Claim 1 wherein:

a plurality of first ground leads is attached to the top surface of the heat sink;

a plurality of second ground leads is attached to the top surface of the heat sink;

the first and second ground leads are segregated into pairs, with the first and second ground leads of each pair being arranged in aligned, spaced relation to each other; and

the first and second ground leads of each pair are disposed between a corresponding adjacent pair of the leads.

5. The semiconductor package of Claim 4 wherein:

a plating section is applied to the top surface of the heat sink;

the semiconductor die is conductively connected to the plating section by at least one of the ground wires;

the first ground lead of each pair is conductively connected to the plating section by at least two of the ground wires; and

the second ground lead of each pair is conductively connected to the plating section by at least one of the ground wires.

6. The semiconductor package of Claim 5 wherein the plating section includes:

a first region which extends between the semiconductor package and the first ground lead of each set, the semiconductor die being conductively connected to the first region;

a third region which extends between the first and second ground leads of each set, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and

at least one second region which extends between and is integrally connected to the first and third regions.

7. The semiconductor package of Claim 6 wherein the plating section includes a plurality of second regions which extend between the first and third regions thereof.

8. The semiconductor package of Claim 1 wherein:

a plating section is applied to the top surface of the heat sink;

the semiconductor die is conductively connected to the plating section by at least one of the ground wires;

the first ground lead is conductively connected to the plating section by at least two of the ground wires; and

the second ground lead is conductively connected to the plating section by at least one of ground wires.

9. The semiconductor package of Claim 8 wherein:

the first and second ground leads are arranged in aligned, spaced relation to each other; and

the plating section includes:

a first region which extends between the first ground lead and the semiconductor die, the semiconductor die being conductively connected to the first region;

a third region which extends between the first and second ground leads, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and

at least one second region which is integrally connected to and extends between the first and third regions.

10. The semiconductor package of Claim 9 wherein the plating section includes a plurality of second regions which extend between the first and third regions thereof.

11. The semiconductor package of Claim 9 wherein the first region of the plating section circumvents the semiconductor die.

12. The semiconductor package of Claim 1 wherein the bottom surface of the heat sink is exposed in the package body.

13. The semiconductor package of Claim 12 wherein the bottom surface of the heat sink is generally planar and is substantially flush with a generally planar exterior surface of the package body.

14. The semiconductor package of Claim 1 further comprising a ring extending between the first ground lead and the semiconductor die.

15. A semiconductor package comprising:

a heat sink having opposed top and bottom surfaces and defining a peripheral edge;

a semiconductor die attached to the top surface of the heat sink;

at least one first ground lead attached to the top surface of the heat sink in spaced relation to the semiconductor die;

at least one second ground lead attached to the top surface of the heat sink in spaced relation to the first ground lead;

a plurality of ground wires conductively connecting the semiconductor die, the first and second ground leads, and the heat sink to each other; and

a package body at least partially encapsulating the heat sink, the semiconductor die, the first and second ground leads, and the ground wires such that at least a portion of the second ground lead is exposed in the package body.

16. The semiconductor package of Claim 15 further comprising:

a plurality of leads extending at least partially about the semiconductor die;

the semiconductor die being electrically connected to at least one of the leads.

17. The semiconductor package of Claim 16 wherein:

a plurality of first ground leads is attached to the top surface of the heat sink;

a plurality of second ground leads is attached to the top surface of the heat sink;

the first and second ground leads are segregated into pairs, with the first and second ground leads of each pair being arranged in aligned, spaced relation to each other; and

the first and second ground leads of each pair are disposed between a corresponding adjacent pair of the leads.

18. The semiconductor package of Claim 17 wherein:

a plating section is applied to the top surface of the heat sink;

the semiconductor die is conductively connected to the plating section by at least one of the ground wires;

the first ground lead of each pair is conductively connected to the plating section by at least two of the ground wires; and

the second ground lead of each pair is conductively connected to the plating section by at least one of the ground wires.

19. The semiconductor package of Claim 15 wherein:

a plating section is applied to the top surface of the heat sink;

the semiconductor die is conductively connected to the plating section by at least one of the ground wires;

the first ground lead is conductively connected to the plating section by at least two of the ground wires; and

the second ground lead is conductively connected to the plating section by at least one of the ground wires.

20. The semiconductor package of Claim 19 wherein:

the first and second ground leads are arranged in aligned, spaced relation to each other; and

the plating section includes:

a first region which extends between the first ground lead and the semiconductor die, the semiconductor die being conductively connected to the first region;

a third region which extends between the first and second ground leads, the first ground lead being conductively connected to the first and third regions, with the second ground lead being conductively connected to the third region; and

at least one second region which is integrally connected to and extends between the first and third regions.